Next, while more than one integrated circuits are failed before a specific testing time in which is corresponding to the knee point, it usually is necessary to perform an optimizing process that deletes part of testing records and performs corresponding processes. While only one integrated circuit is failed before a specific testing time in which is corresponding to the knee point, the specific testing time is a best testing time of these integrated circuits.

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Amended) A method for determining failure rate and selecting a best burn-in time, comprising:

providing a plurality of integrate circuits;

performing a life-time testing process, wherein a failure rate testing time relation is established by measuring the life-time of each said integrated circuit under a testing environment, wherein an acceleration factor function also is established under said testing environment, said acceleration factor function being related to the relationship between a testing time of said testing environment and a real time of a normal operating environment;

performing a simulating process, using a testing time function to simulate said failure rate testing time relation;

performing a transforming process, using said acceleration factor function to transform said testing time function into a real time function, wherein a knee point of said real time function corresponds to an operation time which is said best burn-in time; and

performing an integrating process, integrating said real time function through a calculating region to acquire an accumulated failure rate real time function, wherein said calculating region is a region in which said real time is larger than said best burn-in time.

Please amend claim 2 as follows:

2. (Amended) The method of claim 1, wherein said failure rate testing time relation is divided into three periods in accordance with value of said testing time, said three periods are a infant mortality period, a normal life period and a wear out period.

Please amend claim 9 as follows:

9. (Amended) The method of claim 1, wherein said simulating process is adjusted to minimize the least squares between said failure rate testing time relation and said testing time function.

Please amend claim 10 as follows:

10. (Amended) The method of claim 1, wherein said simulating process is adjusted to minimize the difference between said failure rate testing time relation and said testing time function.

Please amend claim 11 as follows:

11. (Amended) The method of claim 2, wherein said integrating process is stopped while said testing time is located in said wear out period, said testing time being corresponding to said real time.

Please amend claim 12 as follows:

12. (Amended) A method for determining failure rate and selecting best burn-in time, comprising:

providing a plurality of integrate circuits;

performing a life-time testing process, wherein a failure rate testing time relation is established by measuring the life-time of each said integrated circuit under a testing environment, wherein an acceleration factor function also is established under said testing environment, said acceleration factor function being related to the relationship between a testing time of said testing environment and a real time of a normal operating environment;

performing a transforming process, using said acceleration factor function to transform said failure rate testing time function into a failure rate real time function,

performing a simulating process, using a real time function to simulate said failure rate real time relation, wherein a knee point of said real time function corresponds to an operation time which is a best burn-in time for testing said integrated circuits; and

performing an integrating process, integrating said real time function through a calculating region to acquire an accumulated failure

Cont'd A13

rate real time function, wherein said calculating region is a region in which said real time is larger than said best burn-in time.

Please amend claim 16 as follows:

A14

16. (Amended) The method of claim 12, wherein said simulating process is adjusted to minimize the difference between said failure rate real time relation and said real time function.

Please amend claim 18 as follows:

18. (Amended) The method of claim 13, wherein said integrating process is stopped while said testing time is located in said wear out period, said testing time being corresponding to said real time.

A15

[Please amend claim 19 as follows:]

19. (Amended) A method for determining failure rate and selecting best burn-in time, comprising:

providing a plurality of integrate circuits;

performing a life-time testing process, wherein the life-time of each said integrated circuit is measured under a testing environment and then a failure rate testing time relation is established in accordance with a plurality of testing records, wherein an acceleration factor function also is established under said testing environment, said acceleration factor function being related to the relationship between a testing time of said testing environments and a real time of a normal operating environment;

performing a simulating process, using a testing time polynomial of said testing time to simulate said failure rate testing time relation;

performing an optimizing process, part of said testing records are deleted and said corresponding processes are performed again while more than one said integrated circuits are failed before a specific testing time in which is corresponding to a knee point of said testing time polynomial, and said specific testing time is a best testing time of said integrated circuits while only one of said integrated circuits is failed before said specific testing time;

performing a transforming process, using said acceleration factor function to transform said specific testing time into a specific real time and also transform said testing time polynomial into a real time polynomial, wherein said specific real time is a best burn-in time for testing said integrated circuits; and

performing an integrating process, integrating said real time function through a calculating region to acquire an accumulated failure rate real time function, wherein said calculating region is a region in which said real time is larger than said best burn-in time.

Please amend claim 20 as follows:

20. (Amended) The method of claim 19, wherein said integrating process is stopped while said testing time is located in said wear out period, said testing time being corresponding to said real time.

IN THE ABSTRACT:

Please delete the Abstract and substitute therefor the following new Abstract:

The invention comprises the following steps: provide numerous integrate circuits; performs a life-time testing process, wherein a failure rate testing time relation is established by measuring the life-time of each integrated circuit under a testing environment, wherein an acceleration factor function is established under the testing environment; performs a simulating process that a testing time function is used to simulate the failure rate testing time relation; performs a transforming process by using the acceleration factor function to transform the testing time function into a real time function, wherein a knee point of the real time function corresponds to the best burn-in time; and performs an integrating process to integrate the real time function through a calculating region to acquire an accumulated failure rate real time function, wherein the calculating region is a region in which the real time is larger than the best burn-in time.